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8 CORP., MATROX TECH, INC., and
   AEROFLEX COLORADO SPRINGS, INC.
9
                    UNITED STATES DISTRICT COURT
10
                   NORTHERN DISTRICT OF CALIFORNIA
11
                       SAN FRANCISCO DIVISION
12

13

RICOH COMPANY, LTD.,	Case No. C03-4669 MJJ (EMC)
Plaintiff,	Case No. C03-2289 MJJ (EMC)
vs.	**REPLY MEMORANDUM IN SUPPORT OF MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT (RTL)**
AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC.	**[SUMMARY JUDGMENT MOTION NO. 1]** Date: September 26, 2006 Time: 9:30 a.m. Courtroom: 11, 19th Floor Judge: Martin J. Jenkins
Defendants.	
SYNOPSYS, INC.,	
Plaintiff,	
vs.	
RICOH COMPANY, LTD.,	
Defendant.	

27

              FILED UNDER SEAL PURSUANT TO PROTECTIVE ORDER
28   **REDACTED PUBLIC VERSION**

Case Nos. C03-4669 MJJ (EMC) and C03-2289 MJJ (EMC)
REPLY IN SUPPORT OF SUMMARY JUDGMENT RE NON-
INFRINGEMENT [MOTION NO. 1]

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Case Nos. C03-4669 MJJ (EMC) and C03-2289 MJJ (EMC)   -i-
REPLY IN SUPPORT OF SUMMARY JUDGMENT RE NON-
INFRINGEMENT [MOTION NO. 1]

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1 **I.   INTRODUCTION**

2   Ricoh's Opposition to Synopsys' and Defendants' Motion for summary judgment on the issue

3 of whether or not the inputs at issue in this case are "architecture independent" is primarily comprised

4 of arguments lifted verbatim or almost verbatim from its Claim Construction briefs. Here, however,

5 Ricoh disingenuously portrays its claim construction arguments as "factual disputes." In each case, the

6 arguments Ricoh makes (and those arguments made by Dr. Papaefthymiou, Ricoh's hired expert who

7 has never even used Design Compiler or looked at a whole Customer Defendant design)[1] have already

8 been rejected by this Court and should also be rejected here.

9   Moreover, as explained below, not a single disputed fact is raised by Ricoh's motion.   For the

10 reasons set forth in detail below, this Motion should be granted.

11 **II.   THERE ARE NO FACTUAL DISPUTES**

12   Ricoh's alleged disputed "factual" issues are entirely disingenuous wolves in sheep's clothing.

13 The alleged factual issues, and in particular the dispositive issue, alleged factual issue number 1, either

14 consist of an exact re-hash of the legal arguments Ricoh made during claim construction that were

15 already definitively rejected by this Court, or depend on the outcome of an alleged factual issue that is

16 really a legal issue that has already been rejected by this Court, or consist of one of Ricoh's straw man

17 arguments that are quite prevalent throughout its oppositions to this Motion.

18   **A.   Alleged Factual Issue 1 Is Simply An Already Rejected Rehash of Ricoh's Claim**

19   **Construction Arguments**

20   Ricoh's first alleged factual dispute is "What the Darringer '435 Patent teaches about the RTL

21 input to the system disclosed therein." Opposition at 4:17. Ricoh's position is that "Darringer RTL" is

22 a structural level, hardware architecture dependent input that is a shorthand (or straightforward)

23

24 _____

25 [1] On August 11, 2006, Dr. Papaefthymiou testified he has never used Design Compiler; has no idea what inputs Design Compiler requests; had not seen a single Customer Defendant design 11 days prior to his deposition; had never seen the HDL Operators Search Report that formed the basis for his opinion that evidenced all the actions and conditions; had never

26 "read" any of the Customer Defendant transcripts that Ricoh had insisted on; admits that he has no opinion if the Court intended to exclude all RTL; and concedes that his methodology does not even work if applied to the relevant inquiry.

27 Brothers Decl., Ex. 40 (Papaefthymiou) at 18:23-19:5, 66:17-22, 75:6-24; 99:22-100:15, 124:18-125:3, 171:14-172:3, 175:8-22; 180:23-181:15.

28

1   representation of logic." Opposition at 5:1-2. This alleged factual issue consists of nothing more than

2   a rehash of arguments already rejected by the Court in its claim construction. Indeed, in many cases,

3   the arguments are verbatim – or near verbatim – arguments lifted from its Claim Construction briefs,

4   and dropped into Ricoh's Opposition in support of this alleged factual dispute as well as into Dr.

5   Papaefthymiou's declaration/expert report. A detailed comparison of the arguments makes this point

6   abundantly clear.

7   In its opposition to this Motion, Ricoh makes the following assertions in support of its alleged

8   "factual dispute":

9   "[T]he '432 patent describes architecture specific hardware components as part of
10   structural (i.e., "logic") level descriptions. (Brothers Dec. Ex. 26, '432 Patent at col.3,
         lines 59-67." Opposition at 8:25-27.
11

12   "The Darringer '435 Patent teaches that its RTL is a "register-transfer, flowchart control
         language, of logic functions. (Brothers Dec. Ex.38, Darringer '435 Patent at col. 4, lines
         26-32; *see also Id.* at col. 5, lines 27-38) that undergoes a simple translation to AND/OR
13   logic." Opposition at 8:27-9:2.

14   "The '432 Patent file history is clear that the patent Applicants disclaimed hardware
         architecture dependent inputs, and that the patent Applicants considered the Darringer RTL
15   to be such an input. (Brothers Dec. Ex. 39, '432 File History at 215, 235)." Opposition at
         9:5-7.
16

17   "During the '432 patent prosecution, the patent Applicants described the Darringer '435
         patent as teaching "hardware architecture dependent" inputs. (Brothers Dec. Ex. 28, Claim
18   Construction Order at 11 (citing '432 Patent File History))."2 Opposition at 9:8-11.

19   "The register transfer level flowchart control language of Darringer is expressly described
         at col. 4, lines 26-32 as being a 'register transfer, flowchart-control language, of logic
20   functions to be implemented.'" Opposition at 9:16-18.

21   "As taught in the '432 patent, logic level descriptions are structural level, architecture
         dependent descriptions. (Brothers Dec. Ex. 26, '432 Patent at col. 3, lines 59-67)."
22   Opposition at 9:18-20.

23   "Thus, the '432 Patent prosecution history is also consistent with the position that the
24   register transfer level, flowchart control input taught in Darringer is a structural, logic level
         input that is hardware architecture dependent. (Papaefthymiou Dec. ¶¶ 6, 21; Brothers Ex.
25   39, '432 Patent File History at 215; Brothers Dec. Ex. 38, Darringer '435 Patent at col. 4

26   _____

27   2 This citation to the Court's Claim Construction Order is a sleight of hand technique. Here, and elsewhere, Ricoh
     Opposition cites to the Court's Claim Construction Order instead of underlying documents to try to create the impression
     that the Court sanctioned Ricoh's arguments.
28

1   lines 26-32; *see also* Brothers Dec. Ex. 26, '432 Patent at col. 3 lines 59-67)." Opposition
2   at 9:20-25.

3   "The Darringer '435 Patent. As described *supra,* the Darringer '435 Patent teaches a very
     specific system using a specific type of hardware architecture specific, register-transfer
4   level, flowchart control input, of logic functions. (Brothers Dec. Ex. 38, Darringer '435
     Patent at col. 5, lines 27-38, col. 4, lines 26-32; Brothers Dec. Ex. 7, Papaefthymiou Report
5   at 13-15)." Opposition at 9:26-10:2.

6   "The Darringer Patent cannot be the basis of a clear disclaimer of information that it does
     not teach, and is certainly not a clear disclaimer of what it teaches away from. (*See*
7   *PIN/NIP, Inc. v. Platte Chemical Co.*, 304 F.3d 1235, 1246 (Fed. Cir. 2002) (upholding
     patent claims because prior art reference taught away from the claimed invention); *SanDisk*
8   *Corp. v. Memorex Prods., Inc.*, 415 F.3d 1278, 1286 (Fed. Cir. 2005) (reversing district
     court and finding that patentee's prosecution arguments were not a clear and unmistakable
9   disclaimer of claim scope, and further finding that "[t]here is no 'clear and unmistakable'
     disclaimer if a prosecution argument is subject to more than one reasonable interpretation,
10   one of which is consistent with a proffered meaning of the disputed term."); *id.* at 1287
     (citing *Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1332 (Fed. Cir. 2004)). This
11   is additional evidence that Ricoh's disclaimer of the Darringer Patent did not disclaim
     higher order inputs such as those accused in this litigation." [3] Opposition at 11:3-14.
12

13   "The accused inputs are higher order arithmetic operations and other functions that the
     Darringer '435 patent does not teach as inputs to its system. (Brothers Dec. Ex. 7,
14   Papaefthymiou Report at 13-15; *see also* Section IV.A.2, *supra.*) The accused inputs also
     do not undergo a straightforward translation to AND/OR logic." Opposition at 14:7-11.

15   Review of Ricoh's claim construction briefs makes quite clear that these are precisely the

16   arguments Ricoh raised in the past – and which this Court already has rejected. In its Claim

17   Construction briefs, Ricoh argued:

18   "During prosecution of the '432 patent, the patentee distinguished the invention over
     Darringer et al., asserting that the prior art used an input in the form of a register transfer
19   language (RTL)-level flowchart." CC Opening Brief at 20:4-6.

20
     "In contrast, Darringer et al. discloses using a structurally dependent RTL-level input to
21   describe the behavior of the chip that is to be designed." CC Opening Brief at 20:12-13

22   "The "RTL-level" used in Darringer et al. (as well as other prior art references cited in the
     '432 patent prosecution history) requires the input of a "basic" or "primitive Boolean"-type
23   specification of register inputs, outputs, and timing between registers during a single clock
     cycle of the chip operation. See, e.g., Darringer et al. at 5:27-35." CC Opening Brief at
24   20:14-17.

25
     "Darringer et al. states that this type of RTL-level input is simply translated (in well-
26   known manner) into an initial implementation of AND/OR logic by replacing input RTL

27   _____
     [3] Ricoh's claim that these citations are "additional evidence" is ridiculous.
28

1   constructs with their equivalent AND/OR implementations. Id. at 5:35-47." CC Opening
     Brief at 20:17-20:20.
2

3   ". . . the fact that the specification can be so easily (and directly) translated into AND/OR
     logic, indicates that the RTL-level input is a more basic "structural" input." CC Opening
     Brief at 20:22-23.
4

5   "Although [Darringer] can be used to describe the functional aspects of a desired chip, it
     does not do so in a purely higher level functional manner that allows higher level concepts
6   such as addition, multiplication, etc. (or other manner that is free of basic Boolean
     specifications)." CC Opening Brief at 20:24-26.
7

8   "The 'structural' 'RTL-type description utilized in Darringer et al. therefore is not
     'architecture independent.'" CC Opening Brief at 20:26-21:2.
9

10   Ricoh notes that VHDL and Verilog are hardware description languages ("HDLs") used in
     the field of the invention that have been referred to as "RTL-type" languages. This type of
     "RTL-level" is considered to be "functional RTL" as contrasted to the "basic" or
11   "primitive RTL" of Darringer et al." CC Opening Brief at 21:3-8.

12   For any estoppel attributed to the patentee's arguments distinguishing the claimed
     invention over an "RTL"-type input description, it should be made clear that the patentee
13   used the term "RTL" in referring to Darringer et al. (and other prior art systems) that had
     "basic" or "primitive RTL" type of inputs, which were not covered by the '432 patent
14   claims. The patentee did not disclaim coverage, however, of systems that used "functional
     RTL" type of inputs (e.g., VHDL/Verilog based systems) that were architecture
15   independent." CC Opening Brief at 21:9-14.

16   "No such "manifest exclusion" or "clear disavowal" of the scope proposed by
     Defendants is present here. *Sunrace Roots Enter. Co.* v. *SRAM Corp.*, 336 F.3d 1298,
17   1306 (Fed. Cir. 2003) ("To be given effect, such a disclaimer must be 'clear and
     unmistakable.'") (quoting *Omega*, 334 F.3d at 1325). Indeed, "[b]ecause the statements in
18   the prosecution history are subject to multiple reasonable interpretations, they do not
     constitute a clear and unmistakable departure from the ordinary meaning of the [claim term
19   at issue]." *Golight, Inc.* v. *Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1332 (Fed. *Cir.* 2004).
     On this basis alone, Defendants' proposal should be rejected." CC Reply Brief at 6:5-11.
20

21   "Second, and even more egregiously, Defendants make an all-encompassing statement that
     the patentee had added the term "architecture independent" to exclude all register-transfer
22   level (RTL)-type descriptions, as defined in the '435 patent, from the claimed invention,
     selectively quoting the prosecution history. Def Br, at 20. Defendants intentionally omit
23   the actual point of distinction the patentee was making between its claimed invention and
     the '435 patent. The patentee stated: "In order for a designer to utilize the ['435 patent]
24   system, he/she must possess a sophisticated understanding of the complexities of the
     circuit logic itself and therefore have the specialized expert knowledge of a highly skilled
25   VLSI design engineer." April 1989 Amendment at 9. Contrary to Defendants'
     allegation, the patentee did not disclaim all systems using any type of RTL, but only the
26   input system used in the '435 patent, which required knowledge of skilled VLSI design
     engineers in order to provide the level of necessary structural detail. The patentee's use of
27   the term "register-transfer level" or "RTL" was merely a shorthand reference used to
     denote the "structural" RTL-type of input systems prevalent at the time for use in the '435
28   patent." CC Reply Brief at 7:24-8:10.

1   "Indeed, the '435 patent discloses as an input a structural ("technology-oriented") RTL that
     implies a definite structure, and hence, requires a specialized knowledge of hardware

2   design not needed in other types of RTL (e.g., functional RTL). '435 patent at 5:35-38,
     Functional RTI, offers flexibility and adaptability to the designer by eliminating the need

3   for knowledge of structure. For example, unlike in the '435 patent (and other prior art
     cited in the file history), functional RTL allows for the use of operators (e.g.,

4   multiplication, division, etc.) that do not implicate definite structure by the mere input
     description." CC Reply Brief at 8:11-16.

5

6   "The requirement in the '435 patent of specifying the individual inputs, outputs, and
     registers for a single clock cycle, together with the fact that the specification can be so
     easily (and directly) translated into AND/OR logic, indicates that the RTL-level input is a

7   more basic "structural" input. The "structural" RTL-type description utilized in the '435
     patent therefore is not "architecture independent."' CC Reply Brief at 8:17-20.

8

9   A comparison of the quotes from Ricoh's Opposition with the quotes from Ricoh's Claim

10   Construction briefs reveals that there is no question that what they argue in this Opposition are the

11   same exact LEGAL arguments they raised in their Claim Construction briefs.   Indeed the only

12   additions are reliance on an AMI document, which is extrinsic evidence, and in any event not

13   relevant,[4] and more significantly, on Dr. Papaefthymiou's Declaration[5] – which simply reiterates,

14   almost verbatim, Ricoh's arguments.[6] See Papaefthymiou Declaration at ¶5, 7, 13.   Ricoh's efforts to

15   suggest that there is some factual issue were entirely disingenuous and reliant on the assumptions that

16   the Court would allow them to reargue claim construction and that this time their arguments would

17   prevail whereas they had failed before: Ricoh's arguments can be rejected on this basis alone.

18

19

20   _____

21   [4] Ricoh acknowledges that "structural RTL" as used in this document is a special meaning related to replacing specific
     hardware cells in an already mapped netlist which has already been placed and routed, and is therefore irrelevant. Opp. at
     18.

22   [5] Ricoh's reliance on the Darringer thesis does not transform the issues raised from claim construction issues to factual
     issue. Ricoh has long known of the Darringer's patent's citation to the thesis, but never raised it before now. In any event,

23   the single line that Dr. Papaefthymiou points to in the thesis does not change the definition of RTL, but instead the thesis
     defines RTL consistently with the patent.

24   [6] Ricoh's reliance on Dr. Papaefthymiou to rehash these arguments is astounding, given the vigor with which Ricoh

25   objected to any extrinsic evidence in the context of the claim construction proceedings. Moreover, Dr. Papefthymiou's
     deposition transcript – and the Darringer reference itself -- demonstrate the totally disingenuous nature of his unequivocal

26   claims about a simple translation. An expert's opinions must be supported by the evidence. *See General Elec. Co. v.
     Joiner*, 522 U.S. 136, 146 (1997) (expert's opinion excluded where there is too great an analytical gap between the data

27   studied and the opinion proffered). Self-serving declarations that are uncorroborated and contradicted by other evidence do
     not create genuine issues of material fact. *See Johnson v. Washington Metropolitan Area Transit Authority*, 883 F.2d 125,

28   128 (D.C. Cir. 1989); *Villiarimo v. Aloha Island Air, Inc.*, 281 F.3d 1054, 1061 (9th Cir. 2001).

1   Indeed, the Court already rejected each and every argument Ricoh makes with regard to this

2 alleged "factual dispute."[7] In its Claim Construction Order, the Court fully addressed all the issues

3 Ricoh raises. The Court first reiterated Ricoh's argument "Ricoh responds that the patentee's use of

4 the term 'register transfer level' was merely a shorthand reference used to denote the "structural" RTL-

5 type, as opposed to the "functional" RTL-type, of input systems prevalent at the time." Claim

6 Construction Order at 11:28-12:3. The Court then went on to address and reject the arguments raised

7 above as follows:

8
> In order to make this determination, the Court must examine the Darringer 4,704,435
9 Patent ("the '435 patent") and how closely it reads on the present invention. The '435
> patent specifically defines a register-transfer level description and the subsequent
> translation or transformation steps do not alter this express definition.[7] '435 Col. 5:27-38.
10 CC Order at 12:4-7 [Footnote from original]

11 The passage cited in the explicit definition footnote includes the line that reads: "At step 102 in Fig. 2,

12 the register-transfer level description undergoes a simple translation to an initial implementation of

13 AND/OR logic." However, from the context, it is exceedingly clear that the Court is saying, in its

14 order, that the described subsequent translation or transformation steps do not alter the express

15 definition of register-transfer level already set forth.   Indeed, this sentence starts with "[t]he register

16 level description," obviously referring to the register-transfer level description described on the

17 preceding lines.

18   The Court's Order continues, as follows:

19
> The Court finds no relevant distinction between the RTL described in the '435 patent and
20 the RTL specifically disclaimed by in the April and November 1989 Amendments.
> Furthermore, an examination of the '432 patent's public record fails to provide any support
21 for Ricoh's distinction between "structural" and "functional" RTL-type input systems.
> Given these findings, Ricoh's attempts to limit the patentee's disclaimer to only
22 "structural" level RTL-type input systems is unpersuasive. *See Kumar v. Ovaonic Battery
> Co., Inc.* 351 F.3d 1364, 1368 (Fed. Cir. 2003) (adopting definition of term Opposition at
23 d in prior art which is intrinsic evidence). Accordingly, the prosecution history indicates
> that the patentee expressly disclaimed *all register transfer-level descriptions.* CC Order at
24 12:7-15 (emphasis added).

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1   There is no ambiguity in this Order. The Court clearly determined that patentee disclaimed all

2   register-transfer level descriptions, and separately, has definitely rejected the precise arguments Ricoh

3   has re-cast here as alleged "factual" arguments.[8] Resolution of this Motion should begin and end here

4   as there is no dispute that the Customer Defendant inputs are RTL.

5   **B.   Resolution of Alleged Factual Issue No. 1 Resolved Alleged Factual Issue Number**

6   **2**

7   Resolution of this first issue is determinative of factual issue No. 2. Indeed, reaching the

8   second alleged factual issue depends on the ignoring the Court's Claim Construction on the first issue.

9   Indeed, Ricoh asserts in Issue No. 2 that accused inputs are not those taught in the Darringer patent

10   exclusively on the basis of the claim construction it asserted and lost at the claim construction hearing.

11   Ricoh attempts to create confusion by suggesting in footnote 17 that there is a separate issue

12   about whether or not latches are specified in the Customer Defendant inputs. This issue too, however,

13   simply comes down to the already decided claim construction. Specifically, Ricoh's theory here

14   (reiterated in alleged factual issue No. 5) depends on the Court agreeing that Darringer RTL excludes

15   inferring elements of the circuit from specified inputs. Indeed, both Ricoh's argument (Opposition at

16   14, fn.17) and Dr. Soderman's opinion (at ¶53) begin by saying: "[i]nference" or "inferring" includes

17   the use of higher order functional descriptions (rather than structural descriptions)." Thus, Ricoh's

18   argument about inferring is identical to its arguments about arithmetic operators (such as +) – the

19   "always" statement in an input that infers a register is a "higher level" and "not structural" input and

20   thus is precluded from being Darringer RTL. For the reasons set forth above, the Court has already

21   rejected this argument. It should be rejected for the additional reason that this inference does not occur

22   by virtue of some magical event purely inherent in the software, but rather, specific code to infer a

23   register is included by the designer in the input. A hardware designer must specify input

24

_____

25   [8] Ricoh's only mention of anything relating to the Court's order is as follows: "Ricoh understands that the Court's claim
construction analysis states that it did not find a distinction between "structural RTL" and "functional RTL," because the

26   Court could not determine what if any meaning those terms had; however, it was clear that Ricoh had disclaimed the
Darringer RTL input." Nothing in the Court' order suggests that the Court could not determine what if any meaning the

27   terms "structural RTL" or "functional RTL" had. Instead, the Court clearly digested and responded to each of Ricoh's
arguments, and rejected them in its holding that the patentee disclaimed all RTL descriptions.

28

1   corresponding to registers. Indeed, Dr. Soderman testified that the input "always@posclkedge" infers

2   (specifies) a flip-flop, which serves as a register or memory device. Soderman Tr. at 79:9-80:13;

3   51:18-21.

4   Moreover, creating RTL inputs that specify registers requires that the user have specialized

5   knowledge regarding VLSI circuit design. Indeed, Dr. Soderman filed a patent application in 1997

6   directed to system for converting high-level programming language into a "register transfer level

7   (RTL) hardware description language hardware description language that can be synthesized into a

8   gate level hardware representation." De Mory Decl., Ex. 9 at 4:12-14. [9]   Dr. Soderman's patent

9   indicates that there is a need for such a system because "HDLs are specific computer aided design

10   tools for hardware designers . . . . Id. at 1:52-53. The patent goes on to describe the difficulty of using

11   such HDLs. *Id.* Verilog and VHDL are included in the list of the HDLs discussed in the patent. *Id.*

12   **C.   Factual Issue Number 3 Is A Ricoh Straw man**

13   Ricoh's alleged factual issue number 3 is "Whether defendants use of the term 'RTL' to

14   describe their inputs means that their inputs are excluded from the scope of the '432 patent is a straw

15   man argument" As the Court is well aware from Defendants' opening papers, Defendants do much

16   more than claim that use of the term "RTL" means that their inputs do not infringe

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23   [9] Ricoh claims that Defendants have not provided or cited to the Soderman papers and patent or explained the significance
     of these documents. Both statements are false. Defendants have provided Ricoh with information about the patent
24   application and articles. They are Exhibits 17-20 to the August 18, 2006 De Mory Declaration. Exhibit 17 is U.S. Patent
     No. 6,226,776, entitled "System for Converting Hardware Designs in High-Level Programming Language to Hardware
25   Implementations." Exhibit 18 is a 1998 On-Chip System Design Conference article by Donald Soderman, et al, entitled
     "Implementing 'C' Designs in Hardware: A Full-Featured ANSI C to RTL Verilog Compiler in Action." Exhibit 19 is a
26   1998 IEEE article by Donald Soderman and Yuri Panchul entitled "Implementing C Designs in Hardware: A Full-Featured
     ANSI C to RTL Verilog Compiler in Action." Exhibit 20 is a 1998 IEEE article by Donald Soderman and Yuri Panchul
27   entitled "Implementing C Algorithms in Reconfigurable Hardware using C2Verilog." Defendants have also explained the
     inconsistencies in these papers and the patent with the position Ricoh takes here. Opening RTL Brief at pg. 10 fn. 6.
28

1   Because the inputs do and must include this information as defined in Darringer, Defendants

2 contend that their input is RTL.

3   The documents cited in Defendants brief simply corroborate this fact, as well as confirm

4 Ricoh's knowledge of it. Moreover, the documents do not, as Ricoh argues and Dr. Papaefthymiou

5 opines, support the argument that RTL is subject to various interpretations.

6

7

8

9   Instead, at best, the

10 documents evidence that from time to time, different adjectives – all referring to the same inputs with

11 the same characteristics as Darringer and the Customer Defendants designs – are sometimes used with

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16   Indeed, most of the excerpts that Ricoh has selected to include in its brief consistently describe

17 RTL, as the name implies, as specifying registers, and specifying the functions between the registers,

18 and the clock. (The remainder are silent on the details, but are not inconsistent).

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26 [10] Ricoh's reliance on Mr. Andelman's e-mail is a sign of desperation, The reference to "define RTL" in Mr. Andelman's
     e-mail related solely to whether or not it made sense, in the context of third party subpoenas, to try to arbitrarily define RTL
     to encompass all documents that related to the Court's definition of "architecture independent." The goal of arbitrarily
27 redefining RTL was to make sure that the responses to the subpoena's to the universities at which Dr. Papaefthymiou has
     taught would capture all potentially impeaching documents. *See* Docket No. 603.
28

1

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4   In each

5   case, these witnesses are clear – RTL implies a set architecture and set structure of the circuit.[11]

6   Ricoh then goes on to argue the context of the Darringer and '432 patents – again. Opposition

7   at 19-20. This repeated argument once again changes nothing. Ricoh also goes on to make an

8   unsupported or supportable argument that "As used today, some engineers use the label "RTL" very

9   broadly to encompass any input description written in an HDL language." There is absolutely no

10 evidentiary support for this proposition as evidenced by the lack of a single citation in this section of

11 Ricoh's brief. Opposition at 20.

12   Finally, Ricoh claims that Dr. Soderman did not admit that Defendants' inputs are "Darringer

13 RTL."

14

15

16

17   Brothers

18 Decl., Ex. 32 (Soderman) at 77:21-78:1, 108:2-9, 80:1-13, 89:14-90:5. This is a description of RTL.

19   There are no factual disputes raised in this section.

20 **D.**   **Ricoh's Alleged Factual Dispute 5 Is A Red-Herring That Synopsys Believed Ricoh**

21   **Had Abandoned Long Ago**

22   In its introduction in the Opposition, Ricoh claims a fourth factual dispute, "Whether the

23 accused inputs, even if not Darringer RTL, are architecture independent." Ricoh claims that the

24 alleged factual dispute is whether the accused inputs are Darringer RTL and are architecture

25 _____

26 [11] Indeed, there is also no dispute that Design Compiler would not work for purposes of design an ASIC if this information
    is not specified. If one input just a "+" or a "-" or even C=A+B, into Design Compiler, without also including the
27 information required in the RTL definition, no output would result. Indeed, as Dr. Casavant explained, Design Compiler
    counts on the timing behavior of the input as specified by the RTL to match the timing behavior of the output.
28

1 independent, and asserts that the accused inputs are not hardware architecture dependent. Ricoh,

2 however, appears to have abandoned this argument. In any event, as described below, the inputs are

3 architecture dependent.

4   With regard to alleged factual dispute No. 5, if the Court finds the inputs are RTL, which the

5 patentee excluded from its patent scope, then the Court need not even reach this issue (and in fact has

6 decided this issue because RTL implies a set architecture). Even if the Court reaches this issue – it is a

7 red herring. In some Synopsys documentation, such as the single supporting document cited in

8 Ricoh's brief, a 1997 DesignWare technical bulletin, implementation, meaning a particular type of cell,

9 such as a ripple carry adder or a carry look ahead adder, are referred to as "architectures." That

10 implementations are sometimes called architectures has nothing to do with whether or not the inputs

11 specify the architecture of a portion of a circuit or circuit segment. There is no evidence that supports

12 how or why this use of the term as representing an implementation shows that the inputs are

13 architecture independent. Indeed, Dr. Soderman's declaration is the only cited support for this

14 proposition, but it also explicitly depends on the notion that "inferring" "includes the use of higher

15 order functional descriptions (rather than structural descriptions) that Design Compiler ultimately maps

16 to implementations or architectures." Soderman Declaration at ¶53.

17   **E.   Ricoh's Arguments Are Inconsistent And Inconsistent With The '432 Patent**

18   The arguments Ricoh makes here and sworn statements Ricoh makes in response to Motion

19 No. 2, albeit wrong for reasons not significant here, are inconsistent with each other in a manner that is

20 significant to this Motion. In particular, in support of its argument that "hardware cells" can be

21 primitives, Ricoh argues that the cell library in the preferred embodiment is described as containing,

22 among other things, "functional level information: description of the cell at the RTL level." In an

23 attempt to push the square peg of Design Compiler into the '432 round hole, Ricoh asserts that this

24 element is met by the Customer Defendant Technology Libraries. Ricoh's example is an "OR gate

25 (OR2)." Ricoh claims the this "functional RTL level" description of the OR2 cell is met by the

26 functional description (A+B). What Ricoh fails to tells the Court in its brief, however, is that the + in

27 this description is an OR, not something signifying addition. Dr. Soderman, however, confirms this.

28 In footnote 2 to his declaration he states , "As used in this functional description, the "+" represents the

1   Boolean operation OR rather than the arithmetic operation of addition." Soderman at ¶26, fn. 2.

2   Under no circumstances can Ricoh reconcile this sworn testimony and the arguments here that, for

3   purposes of infringing the hardware cell element a Boolean OR is a functional RTL description, but

4   that a Boolean OR in the input to Darringer is unequivocally not functional – but is instead structural

5   RTL!

6   Similarly, in Opposition to Motion 2, Ricoh argues that a "hardware cell" can be a primitive

7   based on Dr. Soderman's sworn testimony that the Negate(A) macro, described as A=NOT(A), would

8   be implemented by one of ordinary skill in the art using a primitive cell such as a one input NAND

9   gate. Soderman Decl. at ¶28. NOT, however, is included in the list of Darringer inputs that Dr.

10   Papaefthymiou, and now Dr. Soderman, opines simply undergoes a "simple translation to AND/OR

11   gates" and thus *cannot be an architecture independent input.* Indeed NOT in an input, according to

12   Dr. Papaefthymiou, specifies structure! Given that NOT is included in the definitions of architecture

13   independent actions and conditions, it is clear that the inventors did not mean to exclude inputs that

14   just require "simple translation."

15   Moreover, NOT is not alone in the common list of actions and conditions described in both the

16   Darringer patent and the '432 definitions of architecture independent actions and conditions. In

17   addition to NOT, Darringer input includes DECODE; there is a DECODE macro in the '432 patent. In

18   addition to NOT and DECODE, the '432 includes a CMP(A,B) operator, one output of which is

19   whether the inputs are equal. Also, both the macros in '432 patent and the ;435 patent include

20   comparisons to zero; the '432 patent has the CMP0 macro, and Figure 4 of the '435 patent shows a

21   comparison to zero. This commonality directly and unequivocally undermines Dr. Papaefthymiou's

22   theory about the "meaning of architecture independent." It would mean that many of the macros (and

23   in fact more than just the explicitly common macros) are really *definitions of architecture dependent*

24   *actions and conditions* – not definitions of architecture independent actions and conditions.[12]

25   _____

26   [12] Indeed, when asked whether the decode as input to Darringer denoted a "specific structure or architecture, Dr. Papaefthymiou testified that decode "implies the output in the way that it only performs a simple transformation to take it

27   from one to the other, "So, yes, decode is really a structural description. It's a very simple element. Are we speaking with respect to add or multiply? It's a very simple element. Once you have decodes, you're really giving structure and

28   description for all practical purposes. You do a simple transformation and basically end up with a structural element as a

                                                                                           (Continued...)

1 **III.   CONCLUSION**

2   For the foregoing reasons, Synopsys requests that declaratory judgment be entered in its favor

3 that the Design Compiler system is not capable of infringing the '432 patent and the Customer

4 Defendants request that judgment of noninfringement be entered.

5 Dated: September 9, 2006   Respectfully submitted,

6   HOWREY LLP

7

8   By: _____ /s/Denise M. De Mory _____

9   Denise M. De Mory
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11   ELECTRONIC SYSTEMS, LTD., MATROX
                                                            GRAPHICS, INC., MATROX INTERNATIONAL
12   CORP., MATROX TECH, INC., and
                                                            AEROFLEX COLORADO SPRINGS, INC.

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26 (...Continued)

27 result of that." Papaefthymiou Tr. at 91:6-23. Thus, according to Dr. Papaefthymiou, the DECODE macro in the
    specification is a definition of an architecture dependent action and condition, as are many of the others.
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